

## Computing Division

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### Equipment Logistics Services

#### 364/364N Dual 4-Fold Logic

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#### GENERAL DESCRIPTION

The Model 364 and 364N are dual 4-fold logic gates which offer the functions of fan-in, coincidence, leading edge inhibit, majority logic, and pulse standardization. Each of two identical channels accepts standard NIM logic signals at each of the four logic inputs and one veto input. All inputs are terminated in 50 Ohm. Lemo-type connectors are used with the single-width Model 364N; BNC type connectors are used with the double-width Model 364.

A front-panel selector allows programming the number of simultaneous negative inputs required for an output. With its majority logic capability, the unit may be used to perform voter coincidence such as 1 of 1, 2, 3, 4 (logic fan-in), 2 of 3, 4, or 3 of 4 as well as the standard coincidences of 2 of 2, 3 of 3, 4 of 4. Any of the inputs serves as an inhibit input when driven with a complementary logic signal. A separate veto input is provided for inhibiting the output regardless of the state of other inputs.

Both channels of the 364 may be gated off by means of the NIM bin gate. The bin gate enters the module via the rear multipin power connector and a rear-panel On-Off switch. Quiescently at +5 volts, the bin gate must be clamped to ground to inhibit the logic unit. The bin gate is directcoupled, and has rise and fall times of approximately 20 ns.

A front-panel selector is provided for programming the participating inputs. Inserting the programming pins in any of the designated Off positions disables that input and eliminates the necessity of removing input cables. A separate storage location is provided for holding the programming pins not in use.

Once the input coincidence conditions have been satisfied, the Model 364 or 364N generates three double-amplitude NIM fast logic outputs. Each output is provided with two paralleled connectors to enable the signal to be clipped, back-terminated, or fanned-out to two 50 Ohm loads. The positive output, or complement (OUT), is quiescently at a logical one state (-32 mA) and switches to 0 mA (or 0 volts) for the duration of the output. The two negative outputs (OUT) are quiescently at zero and switch to -32 mA (-800 mV if both connectors drive 50 Ohm loads) during an output.

The output duration of each channel is either the time overlap of the signals satisfying the coincidence conditions, or a fixed 3.5 ns.

The minimum pulse pair separation of the Model 364 is under 6 ns for an equivalent CW rate of greater than 160 MHz.

The Model 364 offers non-multiple-pulsing operation to assure unambiguous response to input pulses regardless of their amplitude or duration. The 364 will not produce multiple pulses even with input pulses that substantially exceed the output pulse in duration.



**SPECIFICATIONS**

Number of Channels:	Two, all identical
Input Levels:	NIM logic levels: logical 0, 0 mA +/- 2 mA; logical 1, 16 mA +/- 2 mA.
Input Impedance:	50 Ohm +/- 5%; value of impedance is constant up to the limit input protection for negative inputs.
Input Protection:	5 volt protection for pulses. DC overload characteristics are determined by the 250 mW dissipation limit of the 50 Ohm input terminating resistor.
Input Coupling:	Direct; coupling is independent of input risetime, duration, and rate.
Input Reflections:	Dependent upon input risetime; less than 10% for input signal of 2 ns risetime or greater.
Gate:	Logic unit may be inhibited by application of NIM Bin Gate. Bin Gate enters module via pin of rear multipin connector. Switch located on back panel disconnects 364 from Bin Gate line. Clamping Bin Gate to ground from + 5 volts inhibits. Clamping circuit must sink 3 mA per module. Bin Gate circuit is direct-coupled. Rise and fall times are 20 ns.
Negative Outputs:	Two, both with paralleled connectors driven by common high impedance current source. Quiescently 0 mA, current source switches to - 32 mA during output.
Positive Output:	One, complementary, paralleled connectors, quiescently - 32 mA (- 1.6 mV into 50 Ohm load), switching to zero volts during an output.
Output Duration:	Equal to time overlap of input signals or fixed 4.0 ns, (3.5 ns typical) switch selected.
Output Rise and Fall Times:	1.2 ns typical, 10% to 90%; fall time slightly longer on wider widths.
Output Duration Stability:	Less than 0.1%/°C from 20°C from 60°C.
Coincidence Width:	1 ns up, determined by input pulse duration.
Double Pulse Resolution:	Minimum separation to resolve two pulses is typically under 6 ns.
Maximum Rate:	160 MHz typical, input and output; defined for input signals of - 600 mV, 3 ns FWHM.
Functions:	ANDing, ORing, Majority, Inhibit and Complementary logic. < 20 ps rms.
Multiple Pulsing:	None, one and only one output pulse is produced for each input pulse regardless of input pulse amplitude or duration.
Power Requirements:	+ 12 volts at 115 mA, - 12 volts at 150 mA, 120 VAC at 33 mA; voltages must be regulated to +/- . 1%.
Packaging:	The Model 364, 364N are packaged in conformance with AEC standard for nuclear modules (AEC Report TID 20893 Rev.) Completely compatible physically and electrically with LRS Power Chassis Model 108P, and with any other AEC standard power bin of any manufacturer. Model 364 is single-width module using Lemo-type connectors and Model 364N is double-width module using BNC-type connectors.

For assistance contact [helpdesk@fnal.gov](mailto:helpdesk@fnal.gov).

Information maintained by Mike Behnke; last modified on July 11, 2006.

(Address comments about page to [prep-webmaster@fnal.gov](mailto:prep-webmaster@fnal.gov).)